

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Jc872 U.S. PTO
09/993967
11/27/01

IN RE: PATENT APPLICATION OF

YAMADA et al.

Group Art Unit: Not Yet Assigned

Appln. No.: Not Yet Assigned

Examiner: Not Yet Assigned

Filed: November 27, 2001

Title: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

November 27, 2001

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Attached is a Form PTO 1449 listing the enclosed document.

This Information Disclosure Statement is intended to be in full compliance with the rules, but should the Examiner find any part of its required content to have been omitted, prompt notice to that effect is earnestly solicited, along with additional time under Rule 97(f), to enable Applicant to comply fully.

Consideration of the foregoing and the enclosure plus the return of a copy of the enclosed Form PTO-1449 with the Examiner's initials in the left column per MPEP 609 along with an early action on the merits of this application are earnestly solicited.

Respectfully submitted,

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FORM PTO-1449 (modified)
 To: U.S. Department of Commerce
 (PW FORM PAT-1449)
 Patent and Trademark Office

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JCS72 U.S. PRO
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**INFORMATION DISCLOSURE STATEMENT
 BY APPLICANT**

Date: November 27, 2001

Page **1** of **1**

Applicant: YAMADA et al.

Appln. No.: Not Yet Assigned

Filing Date: Herewith

Examiner: Group Art Unit:

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
AR						
BR						
CR						
DR						
ER						
FR						
GR						
HR						
IR						
JR						
KR						
LR						
MR						
NR						

FOREIGN PATENT DOCUMENTS

	Document Number	Date MM/YYYY	Country	Inventor Name	English Abstract		Translation Readily Available	
					Enclosed	No	Enclose	No
OR								
PR								
QR								
RR								
SR								
TR								
UR								
VR								

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

WR	U. Gruening, et al., IEDM Technical Digest, "A Novel Trench DRAM Cell with a VERTical Access Transistor and Buried STrap (VERI BEST) for 4Gb/16Gb", 1999, pp. 25-28			
XR	C. J. Radens, et al., IEDM Technical Digest, "An Orthogonal 6F2 Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", 2000, pp. 349-352			
YR				
ZR				
AAR				

Examiner

Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.